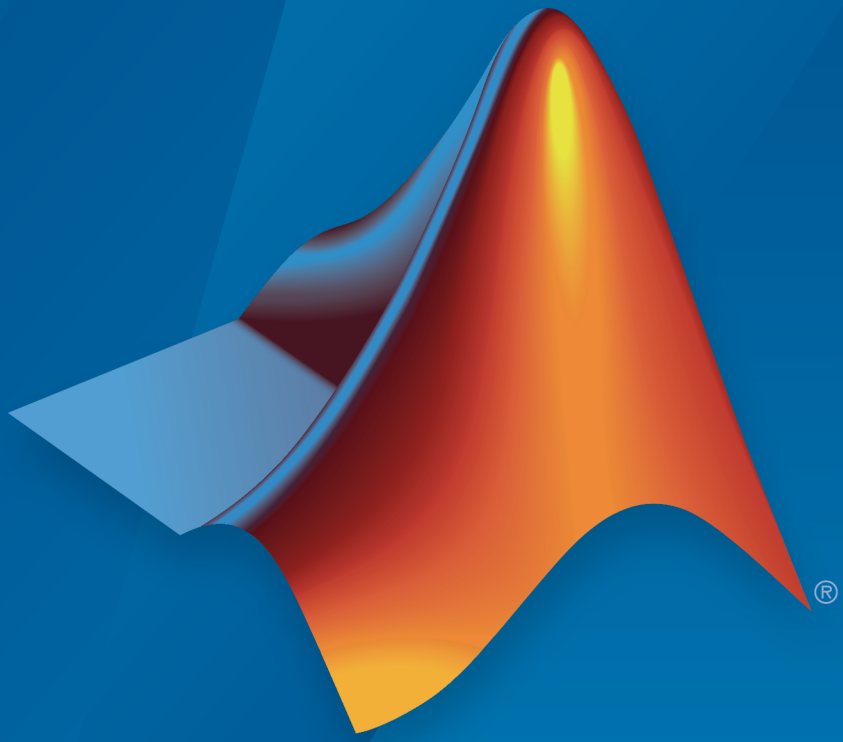
Vision HDL Toolbox™ Release Notes



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The MathWorks, Inc.
3 Apple Hill Drive
Natick, MA 01760-2098

Vision HDL Toolbox™ Release Notes

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R2017a

Version: 1.4

New Features

Bug Fixes

Pixel Stream Aligner: Synchronize two video streams for comparison or overlay

The Pixel Stream Aligner block synchronizes two pixel streams by delaying one stream to match the timing of a reference stream. You can use this block to align streams for overlaying, comparing, or combining two streams, such as in a Gaussian blur operation. Connect the delayed stream as the reference, and the earlier stream to the `pixel` and `ctrl` ports.

This release also includes an equivalent System object™, visionhdl.PixelStreamAligner.

Corner Detection Example: Overlay detected corners using the Pixel Stream Aligner

The “Corner Detection” example is updated to use the Pixel Stream Aligner block to implement the overlay of the detected corners onto the original image.

Lane Detection Example: Process 480p video and compute ego lanes in FPGA

The “Lane Detection” example now accepts 480p input video, without padding. To accommodate the larger birds-eye-view frame, the design does not accept new input while processing the current frame. Input frames that arrive before the previous frame is finished are dropped. The example now determines which detected lanes are the ego lanes, and removes outliers, in hardware.

R2016b

Version: 1.3

New Features

Bug Fixes

Compatibility Considerations

Lane Detection Example: Reference design demonstrating FPGA acceleration of a lane detection algorithm

This example shows FPGA acceleration of lane-marking detection. The design includes an FPGA-based candidate generator and a software-based polynomial fitting engine. See Lane Detection.

Measure Timing Block and System Object: Measure video signal timing from the pixel control bus

Use the Measure Timing block to investigate the blanking intervals between active frames in streaming video data. This block observes the control signals in the pixel control bus in your model, and returns the timing characteristics of the frames.

This release also includes an equivalent System object, visionhdl.MeasureTiming.

AXI4-Stream Video Interface: Generate an HDL IP core with an AXI4-Stream Video interface for your video algorithm (requires HDL Coder)

When your synthesis tool is Xilinx® Vivado®, HDL Coder™ can generate an IP core with an AXI4-Stream Video interface for your video algorithm. To generate an IP core, model your video algorithm using the streaming pixel interface. Then, in the **Target platform interface table**, map the pixel data and pixel control bus ports to the `AXI4-Stream Video Master` or `AXI4-Stream Video Slave` interfaces.

You can integrate the generated IP core into the `Default video system` reference design or your own custom video reference design.

See Model Design for AXI4-Stream Video Interface Generation.

Computer Vision on Xilinx Zynq-Based Hardware: Generate and verify vision algorithms on a prototype board connected to a live HDMI video stream

The Computer Vision System Toolbox™ Support Package for Xilinx Zynq®-Based Hardware (introduced April 2016) supports verification and prototyping of vision algorithms on Zynq-based hardware.

HDL Coder is required for customizing the algorithms running on the FPGA fabric of the Zynq device. Embedded Coder® is required for customizing the algorithms running on the ARM® processor of the Zynq device. Using this support package, you can:

- Target your video processing algorithms to Zynq hardware from Simulink®. This includes support for Vision HDL Toolbox™ blocks.
- Stream HDMI signals into Simulink to explore designs with real data.
- Generate HDL vision IP cores, using HDL Coder. This includes support for algorithms that use Vision HDL Toolbox blocks.
- Deploy algorithms and visualize them using HDMI output on a screen.

For additional information, see Computer Vision System Toolbox Support Package for Xilinx Zynq-Based Hardware.

Optimized grayscale morphology using Van Herk algorithm

The grayscale morphology blocks and objects now implement the Van Herk algorithm for line, square, or rectangle structuring elements with more than 8 columns. This algorithm uses fewer hardware resources, and has higher latency, than the previous comparator tree implementation.

This change affects these blocks and objects:

- Grayscale Closing
- Grayscale Dilation
- Grayscale Erosion
- Grayscale Opening
- visionhdl.GrayscaleClosing
- visionhdl.GrayscaleDilation
- visionhdl.GrayscaleErosion
- visionhdl.GrayscaleOpening

Compatibility Considerations

Due to the latency change, you might need to rebalance parallel path delays in your models that contain morphology blocks. A best practice is to use the pixel stream control

signals to synchronize parallel paths in your models, rather than inserting a specific number of delays.

The latency of a Van Herk kernel for a neighborhood of $m \times n$ pixels is $2m + \log_2(n)$. The block implements this kernel for line, square, or rectangle structuring elements more than 8 pixels wide, with no pixels set to zero.

The latency of a comparison tree kernel for a neighborhood of $m \times n$ pixels is $\log_2(m)+\log_2(n)$. The block implements this kernel for structuring elements smaller than 8 pixels wide, or those with one or more pixels set to zero.

Simpler way to call System objects

Instead of using the `step` method to perform the operation defined by a System object, you can call the object with arguments, as if it were a function. The `step` method continues to work. This feature improves the readability of scripts and functions that use many different System objects.

For example, if you create a `visionhdl.LookupTable` System object named `invertgray`, then you call the System object as a function with that name.

```
invertgray = visionhdl.LookupTable(uint8(linspace(255,0,256));
for p = 1:numPixelsPerFrame
    [pixOut(p),ctrlOut(p)] = invertgray(pixIn(p),ctrlIn(p));
end
```

The equivalent operation using the `step` method is:

```
invertgray = visionhdl.LookupTable(uint8(linspace(255,0,256));
for p = 1:numPixelsPerFrame
    [pixOut(p),ctrlOut(p)] = step(invertgray,pixIn(p),ctrlIn(p));
end
```

When the `step` method has the System object as its only argument, the function equivalent has no arguments. You must call this function with empty parentheses. For example, `step(sysobj)` and `sysobj()` perform equivalent operations.

R2016a

Version: 1.2

New Features

Bug Fixes

ROI Selector: Select a region of interest from a streaming video source

The new block, ROI Selector, selects a region of interest (ROI) from a video stream. You can specify one or more regions using input ports or mask parameters. The block returns each new region as streaming pixel data and corresponding `pixelcontrol` bus.

This release also includes an equivalent System object, visionhdl.ROISelector.

Grayscale Morphology: Perform dilation, erosion, opening, and closing operations on grayscale inputs

Perform grayscale morphology using these new blocks and System objects:

- Grayscale Closing
- Grayscale Dilation
- Grayscale Erosion
- Grayscale Opening
- visionhdl.GrayscaleClosing
- visionhdl.GrayscaleDilation
- visionhdl.GrayscaleErosion
- visionhdl.GrayscaleOpening

Larger frame size for statistics computations

The Image Statistics block and visionhdl.ImageStatistics System object now support input regions up to 64^4 (16,777,216) pixels in size.

R2015b

Version: 1.1

New Features

Bug Fixes

Corner Detection Example: Detect intersecting edges with the Harris algorithm

This example uses the Image Filter block to implement the Harris & Stephens corner detection algorithm. See “Corner Detection” in Vision HDL Toolbox Examples.

MATLAB Compiler Integration: Generate standalone executables for System objects

All System objects in Vision HDL Toolbox support generating executables with MATLAB® Compiler™.

HDL code generation for structure arguments in MATLAB

HDL Coder now supports code generation for structure arguments of functions. For Vision HDL Toolbox, this simplifies the arguments of functions targeted for HDL code generation. Previously, you had to flatten the structure into the component control signals.

```
function [pixOut,hStartOut,hEndOut,vStartOut,vEndOut,validOut] = ...
      HDLTargetedDesign(pixIn,hStartIn,hEndIn,vStartIn,vEndIn,validIn)
```

With HDL code generation support for structures, the arguments can now include the control signal structure.

```
function [pixOut,ctrlOut] = HDLTargetedDesign(pixIn,ctrlIn)
```

The structure becomes individual control signals in the generated Verilog® or VHDL® code.

Improved line buffer performance

This release improves the HDL performance of blocks and objects that have internal line memory. The synthesized HDL code for the line buffer now supports HD video at 60fps on the Xilinx Zynq-7000 ZC702 board, and 4k video at 30fps on the Xilinx Zynq-7000 ZC706 board. The following blocks and System objects use the improved line buffer code:

- Demosaic Interpolator
- Edge Detector
- Image Filter

- Median Filter
- Closing
- Dilation
- Erosion
- Opening

For example, the table shows the R2015b performance of the Demosaic Interpolator, using **Gradient-corrected linear** interpolation, and synthesized with Xilinx Vivado for these target boards.

Xilinx Zynq-7000 ZC702	Xilinx Zynq-7000 ZC706
HD input video	4k input video
200 MHz	375 MHz
Consumes: • no DSP48s • 2.5% of the LUTS • 1.5% of the slice registers • 8 BRAMS (4%)	Consumes: • no DSP48s • 0.6% of the LUTS • 0.4% of the slice registers • 8 BRAMS (1%)

In the previous release, the performance is shown below.

Xilinx Zynq-7000 ZC702	Xilinx Zynq-7000 ZC706
HD input video	4k input video
135 MHz (need 150 MHz for 60 fps)	230 MHz (need 300 MHz for 30 fps)
Consumes: • no DSP48s • 2.6% of the LUTS • 1.5% of the slice registers • 8 BRAMS (4%)	Consumes: • no DSP48s • 0.5% of the LUTS • 0.3% of the slice registers • 8 BRAMS (1%)

R2015a

Version: 1.0

New Features

Video synchronization signal controls for handling nonideal timing and resolution variations

Vision HDL Toolbox blocks and System objects accept and return video data as a serial stream of pixel data and control signals. The protocol mimics the timing of a video system, including inactive intervals between frames. Each block or object operates without full knowledge of the image format, and can tolerate imperfect timing of lines and frames. See Streaming Pixel Interface.

Configurable frame rates and sizes, including 60FPS for high-definition (1080p) video

To support HD video applications, Vision HDL Toolbox blocks and System objects generate HDL code capable of running at 150 MHz.

For supported video formats, see the Frame To Pixels block.

Frame-to-pixel and pixel-to-frame conversions to integrate with frame-based processing capabilities in MATLAB and Simulink

In MATLAB, use the visionhdl.FrameToPixels object to convert framed video data to a stream of pixels and control signals.

In Simulink, use the Frame To Pixels block to convert framed video data to a stream of pixels and control signals.

Image processing, video, and computer vision algorithms with a pixel-streaming architecture, including image enhancement, filtering, morphology, and statistics

Vision HDL Toolbox blocks and System objects implement hardware-friendly architectures. For the list of blocks and System objects provided in this product, see HDL-Optimized Algorithm Design.

Implicit on-chip data handling using line memory

Some Vision HDL Toolbox blocks and System objects include internal memory for a small number of lines as required for the calculation at each image pixel.

The line memory stores *kernel size - 1*-by-*active pixels per line* pixels. Set **Line buffer size** to a power of two that accommodates *active pixels per line*.

Support for HDL code generation and real-time verification

Vision HDL Toolbox provides libraries of blocks and System objects that support HDL code generation. To generate HDL code from these designs, you must have an HDL Coder license. HDL Coder also enables you to generate scripts and test benches for use with 3rd party HDL simulators.

If you have an HDL Verifier™ license, you can use the FPGA-in-the-loop feature to prototype your HDL design on an FPGA board. HDL Verifier also enables you to cosimulate a Simulink model with an HDL design running in a 3rd party simulator.

See HDL Code Generation and Verification